Chapter 2

Overview of Silicon PIN Dectectors

2.1 PIN Diodes

2.1.1 General Discussion of PIN Diodes

A PIN diode is very similar to a PN diode (a pn junction), except that an intrinsic layer[1], sometimes referred to as the bulk of the diode, is placed in between the p and n type materials. PIN diodes are more commonly used in photodetectors than PN diodes since the intrinsic region presents a larger volume in which photons can produce electron-hole pairs and so the thickness of this region can be adapted to increase quantum efficiency. The thickness of this region also gives them a lower capacitance than a typical PN diode. With a forward bias, the PIN diode behaves like a variable resistor for high-frequency signals. With a reverse bias, it acts as a parallel plate capacitor [53].

The most commonly used materials in PIN diodes are Silicon (Si) and Galium Arsenide (GaAs). Since the focus of this thesis is on Si PIN photodiodes, we will refer to Silicon as the relevant material unless otherwise noted. The bulk region of Si PIN detectors is ideally composed of a very high resistivity (ρ) intrinsic silicon. However, in practice this region is doped with slightly n-type, n^- silicon, or slightly p-type, p^- silicon. One usually calls the former a PνN diode and the latter a PπN diode. The main difference between the two is the sign of the space charge density in the bulk region. For the case of the PνN diode, the *ionized*[2] donors will yield a positive charge density while the PπN will have a negative charge density. It follows that the resultant electric field and potential in each will also be different.

A diagram of a PνN diode is shown in the upper portion of Figure 2.1. W is the total width of the intrinsic (or slightly doped) region and A is the cross-sectional area. W_P is the width of the

[1]Intrinsic silicon has the property that, in thermal equilibrium, the number of conduction band electrons per unit volume, n_c is equal to the number of valence band holes, p_v.

[2]The term *ionized* can be confusing for the case of semiconductors. When a donor atom loses its extra electron, it will contribute a net positive charge. When an acceptor atom loses a hole, it will contribute a net negative charge.

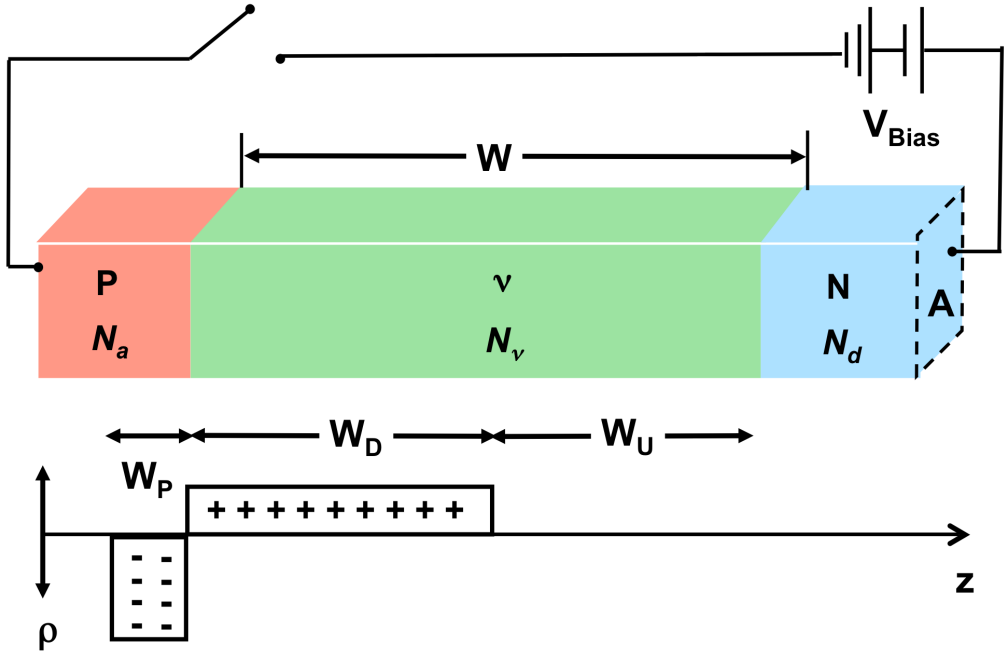

Figure 2.1: The top diagram shows the dimensions and composition of a PIN diode with donor densities of N_d in the N region and N_ν in the ν region, and an acceptor density of N_a in the P region. The cross sectional area is A and the width of the intrinsic region is W. The widths of the depleted and undepleted portions of the lightly doped n^- region are W_D and W_U, respectively. The width of the depletion region in the P material is W_P. Below is a plot of the space charge density due to the ionized donors/acceptors.

depletion region in the P contact, W_D is the width of the depletion region in the intrinsic layer, and $W_U = W - W_D$ is the width of the undepleted, or *diffusion* region in the intrinsic layer. Below the diagram is a rough sketch of the charge density for the case when the switch is open. The open switch is one of three main regimes under which the PIN diode can be operated, as follows.

1. **Open Voltage** : Switch is open

   - Charge carriers will diffuse until equilibrium is reached. In the dark, the voltage across the diode will take a nonzero value , V_{bi}, called the *built-in* voltage.
   - The field is zero near the contacts, so charge conservation demands that $W_P N_A = W_D N_\nu$. Thus, the depletion region extends further into the lightly-doped material than it does into the p material.
   - If illuminated, the voltage will change in proportion to the photon flux. This is known as the *photovoltaic effect*.

2. **Reverse Bias** : Switch is closed, $V_{Bias} > 0$

   - W_D will increase with increasing $|V_{Bias}|$.
   - When $|V_{Bias}|$ reaches a critical value, V_{PT}, called the the *punch-through* voltage, $W_D = W$, and the diode is said to be *fully depleted* of charge carriers. For voltages greater than this, the bulk will be *overdepleted*.
   - An electric field exists in the space charge region. This field will sweep carriers generated by thermal or photon excitation to the edges of the depletion region.
   - For $|V| < V_{PT}$, a diffusion region exists near the νN interface where there is no electric field. Charges created here will wander some typical distance D_B. Most will recombine; some will make it to the edges of the depletion region where they will be collected.
   - At thermal equilibrium, only a small reverse current will flow.

3. **Forward Bias** : Switch is closed, $V_{Bias} < 0$

   - W_D will shrink with increasing $|V_{Bias}|$.
   - At thermal equilibrium, a large current will flow across the diode as carriers are injected. This current is almost entirely due to diffusion of these carriers across the p^+-n junction; not drift. Holes from the p side diffuse to the n side and become minority carriers and electrons from the n side do the same thing on their way to the p side. The current is limited by the recombination of the two species when they become minority carriers on the opposite side.

In photodetection applications, PIN diodes are nearly always operated in reverse bias. However, the case of switching from a forward or zero bias to a reverse bias can cause non-equilibrium effects and difficulty in operating them as photodetectors and cannot be ignored completely. Both cases will be considered in detail in later sections.

2.1.2 PIN Diode Circuit Equivalent Model

One can model the PIN diode as a simple circuit consisting of capacitors and resistors [54]. The circuit equivalent at zero bias is shown in Figure 2.2. The undepleted portion of the intrinsic region is modeled as a capacitor, C_i, in parallel with a resistor, R_i. $C_i = \epsilon A/W_U$ is usually referred to as the diffusion capacitance and accounts for the charge stored in the undepleted portion of the bulk region. $R_i = \rho W_U/A$ is the resistance arising from the high resistivity silicon that has not been depleted in the bulk. In series with this combination, the depleted portion of the bulk contributes a capacitance $C_j = \epsilon A/W_D$ and the N and P contacts have a resistance R_C.

While the value of R_C remains nearly constant for varying values of V_{Bias}, C_J, C_i, and R_i are very dependent on it. As noted in the previous section, when a reverse bias is applied, W_D will

increase and W_U will decrease. Inspection of C_i shows that it will diverge as the bulk becomes fully depleted. However, at the same time the resistance R_i is going to zero. So when $W_D = W$, the parallel component of the circuit can be modeled as a short and the total capacitance of the circuit approaches a constant value of C_j. This is the value that is usually quoted for the capacitance of a photodetector since they are usually operated in full depletion.

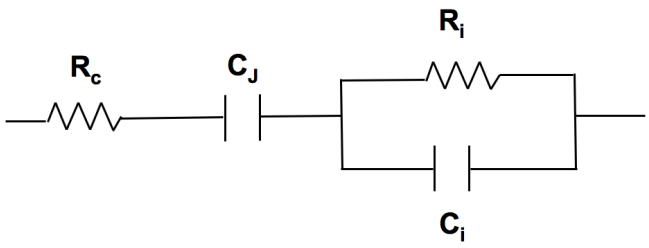

Figure 2.2: Circuit equivalent of a PIN diode. The capacitance, C_i, and resistance, R_i of the intrinsic (or lightly doped region) are in parallel and this portion of the circuit is in series with the junction capacitance, C_j and the contact resistance, R_c.

2.1.3 Punch Trough Voltage

If we apply a large enough reverse bias voltage V_{Bias} to the N side of the diode and fully deplete the bulk of charge carriers, there will be a non-zero electric field extending all the way across it due to the ionized donor atoms. The voltage at which this happens is referred to as the *punch-through* voltage. At a positive voltage less than this, there will be a *diffusion* region near the νN interface in which charge carriers experience no field.

The electric field in the fully depleted region can be approximated by neglecting any transverse fields (i.e. considering this a 1-d problem along the z direction) and applying Gauss's law,

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\epsilon}, \tag{2.1}$$

where ρ is the charge density and ϵ is the relative permittivity of silicon. If we consider the charge distribution as arising purely from the ionized donors, then $\rho(z) = N_\nu(z)$ is a constant in the depletion region and zero in the diffusion region. Integration of Gauss's law then yields the electric field:

$$E(z) = \frac{zN_\nu q}{\epsilon}, \tag{2.2}$$

and integrating this field yields the electric potential (neglecting sign):

$$\phi(z) = \frac{z^2 N_\nu q}{2\epsilon}. \tag{2.3}$$

Assuming that the punch-through voltage has been reached and the bulk has been fully depleted so

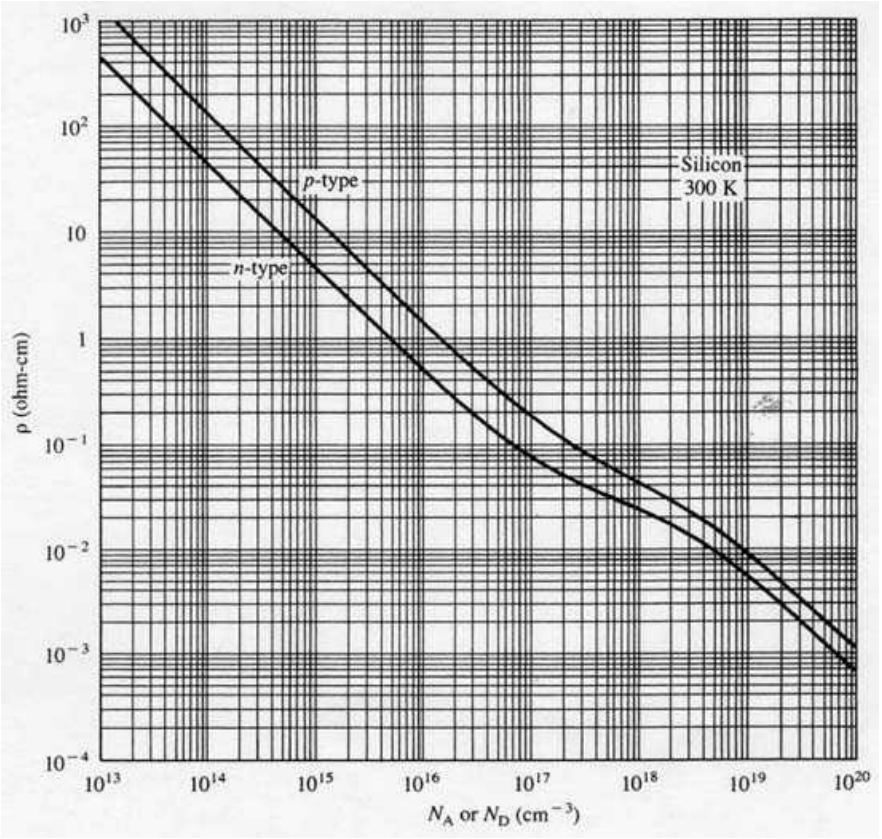

Figure 2.3: A plot taken from [55] showing the resistivity of silicon as a function of doping density.

that $z = W$, we have,

$$V_{PT} = \frac{W^2 N_\nu q}{2\epsilon}. \tag{2.4}$$

Equation 2.4 allows us to calculate the punch-through voltage and reveals the $\sqrt{V}$ dependence of the depletion region width on the reverse bias. However, it does not describe the shape or magnitude of the field in regions where the donors have not been ionized or at the PI and IN interfaces. The latter regions are important as the fields here may dominate charge transport.

Furthermore, this calculation neglects the P and N regions entirely, considering them essentially as metal electrodes. As shown by Figure 2.3, the resistivity of silicon declines to about 10^{-3} Ω·cm at very high doping densities. However, this is still 3 orders of magnitude higher than the resistivity of typical conductors such as copper or silver. The voltage necessary to deplete these regions of their carriers may not be negligible in certain cases.

To describe the fields in the undepleted region and understand the distribution and dynamics of the charge carriers near the interface, it is necessary to solve the equations numerically.

2.2 HyViSI Detector

The detectors studied in this thesis are Hybrid Visible Silicon (HyViSI) CMOS arrays. They consist of two layers: an array of Silicon PIN didoes that serve as the photodetectors and a source follower per detector (SFD) CMOS HxRG multiplexer (where the "x" stands for 1, 2, or 4, depending on the format) that acts as the readout circuit. The two layers are manufactured separately, allowing for independent optimization of photocollection and readout. While many aspects of the optimizations will be covered, the reader is referred to Bai et al. [37, 56, 25] for the exhaustive details.

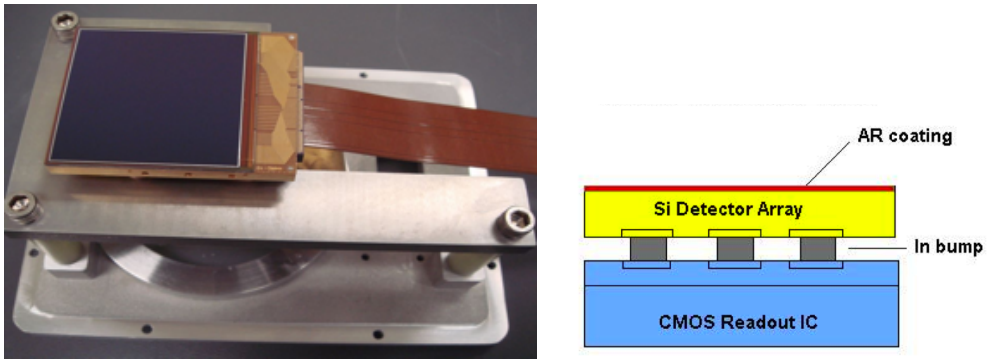

Figure 2.4: (Left) Picture of H4RG HyViSI detector. (Right) Cross section view of HyViSI detectors taken from [37].

Once fabricated, the two layers are precisely aligned so that the pixels of the detector lie directly on top of the pixels in the MUX, as shown in the right of Figure 2.4. They are then "cold welded" together with a pressure of up to several hundred kilograms [23]. After the cold welding, the two layers will be effectively "glued" together by the indium bumps, which also serve as the conductive path between a pixel in the photodector and the mux. As one might imagine, this process is very difficult. Many devices suffer from a large amount of "broken" pixels (the word "broken" will be clarified in Section 4.2). This low yield factor is one of the great challenges that must be met before SiPIN detector arrays become a viable alternative to more conventional imagers. For most devices tested in this thesis work—all 1k×1k H1RGs and 2k×2k H2RGs, but not the 4k×4k H4RG—over 99.9% of the pixels were functional and behave effectively as PIN diodes.

2.2.1 HyViSI PIN Diode

The diodes in the HyViSI detectors possess a bulk region with a width of $W = 100$ μm that is slightly n-type. Thus, when the bulk is depleted the ionized donors in it give rise to a positive space charge density. This slightly doped intrinsic region is sandwiched between highly doped p^+ and n^+ regions, as shown in Figure 2.1. For the purpose of this section, the cross sectional area is assumed

to be that of an entire 10 μm pixel, i.e. $10\mu\text{m} \times 10\mu\text{m} = 100\mu\text{m}^2$. However, the p^+ region does not actually occupy the entire pixel and this fact will be taken into account in later analyses of the detector.

On the n^+ side a substrate voltage called V_{SUB} is supplied with either a power supply or battery. At the p^+ site the voltage is V_{Node}: the same voltage seen at the gate of the unit cell source follower in the multiplexer, the two being coupled by the indium bump bond between them. V_{Node} can be held at V_{RESET} by holding the reset switch or allowed to rise as photocharges swept out of the bulk integrate. If $V_{Node} > V_{SUB}$, the diode is forward biased and if $V_{Node} < V_{SUB}$, it is reverse biased.

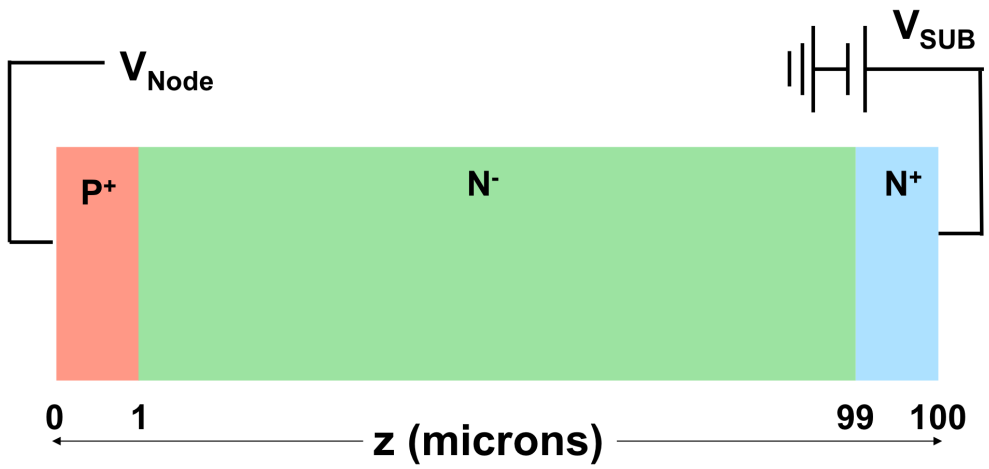

Figure 2.5: Diagram showing the dimensions and composition of the PIN diodes in the HyViSI detector (not to scale). For simplicity, the entire diode is assumed to be 100 μm long. The bulk is slightly n-type material. At the p^+ side, the node voltage V_{node} integrates as holes are collected. The reverse bias is held by V_{SUB} on the n^+ side with a power supply or battery.

In reverse bias, with a thickness of 100 μm and 11.8 as the dielectric constant of silicon, Equation 2.4 yields a punch through voltage of 7.7 Volts. The PIN diodes in the HyViSI devices are typically operated at voltages higher than this to ensure that the bulk is overdepleted. This ensures that the photo-generated charges are swept out of the bulk before recombining, and the higher the value of V_{SUB} is, the less lateral diffusion of charge there will be. However, values of V_{SUB} between zero and V_{PT} are useful in determining characteristics of the detector such as lifetime and diffusion lengths of the charge carriers.

2.2.1.1 Simulation Results

Using the method outlined in Appendix C and guesses for the doping densities in the HyViSI PIN diodes, we have calculated the electric field, carrier densities, and charge densities, for various values

of V_{SUB}. From these quantities we can easily obtain the potential and energy-band diagrams and investigate the band bending near the surfaces, a matter which will be handled in a later section. As a first approximation, the voltage at the integrating node, V_{Node}, is held at ground and the PI and IN interfaces are assumed to be diffused layers with Gaussian-type distributions, giving a doping profile similar to the one modeled in Kurata [57]. The first of these approximations will be refined in later sections to account for the voltage increase due to integration of photo-generated charge at the p^+ nodes.

The simulation is performed with a nonuniform mesh consisting of 4000 points, with closely spaced grid points near the junctions ($\Delta x_i = 1$ nm) and coarsely spaced ones (a maximum of $\Delta x_i \approx 0.26$ μm) in the bulk. The results at steady-state, when the generation and recombination terms are equal at each grid point, are shown in Figure 2.6 for the case where the bulk is not fully depleted and in Figure 2.7 for the case in which the bulk is depleted or overdepleted. There are several interesting features to note in each of these cases.

0-10 Volts: The electric field plots in the top of Figure 2.6 show good agreement with the result of Equation 2.4. For voltages less than $V_{PT} \sim 8$ volts, we see that a region with zero electric field exists in the bulk silicon. In these regions there is a substantial non-zero charge carrier density. We expect holes generated in this region to recombine before making it to the boundary where the amplitude of the electric field starts to increase. These diffusion regions are undesired in photo-detection operation since many of the electron-hole pairs generated by impinging photons will recombine and will not contribute to the signal.

Another interesting feature is the large electric field amplitude at the Pν and νN interfaces. This is to be expected from the large mismatches in doping concentrations at these boundaries and the fact that we demand the electric field vanish at the contacts. In reality, the electric field may have nonzero values due to the fact that the p+ and n+ contacts are not perfect conductors and are in contact with regions that may be hosts to numerous charge traps. Also, in normal operation the p+ region will actually be accumulating minority carrier holes from the bulk, so we expect to modify the boundary condition at $z = 0$ to account for this.

Lastly, at 10 volts we see that a non-zero electric field exists throughout the diode. This indicates that the punch-through voltage has been reached. However, near the n+ we see that the electron carrier density still has a large non-zero value of about 10^{12} cm-3. This indicates that the diode has not reached an overdepleted state; a further increase in V_{SUB} is necessary to reach this regime.

15-35 Volts: After the punch-through voltage has been reached, the diode is said to be in an overdepleted state. Increasing V_{SUB} further reduces the carrier and charge densities near the n+ν boundary. It also increases the magnitude of the electric field throughout the diode. The latter is especially important for increasing CCE and reducing crosstalk.

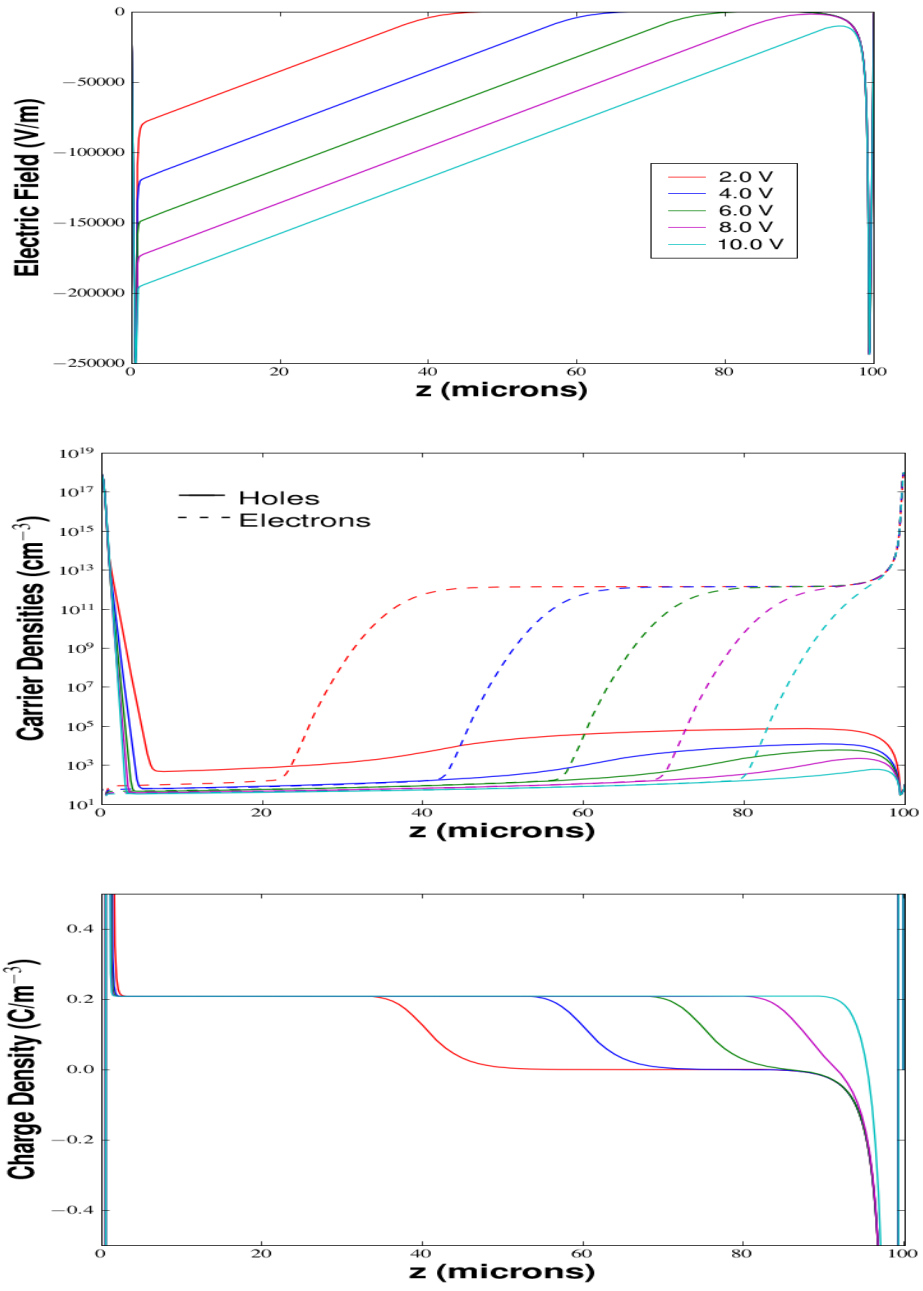

Figure 2.6: Simulated electric field (top), carrier densities (middle), and charge density (bottom) in the HyViSI PIN diodes. For most voltages shown the bulk is not fully depleted. All quantities were obtained through the numerical simulations described in Appendix C.

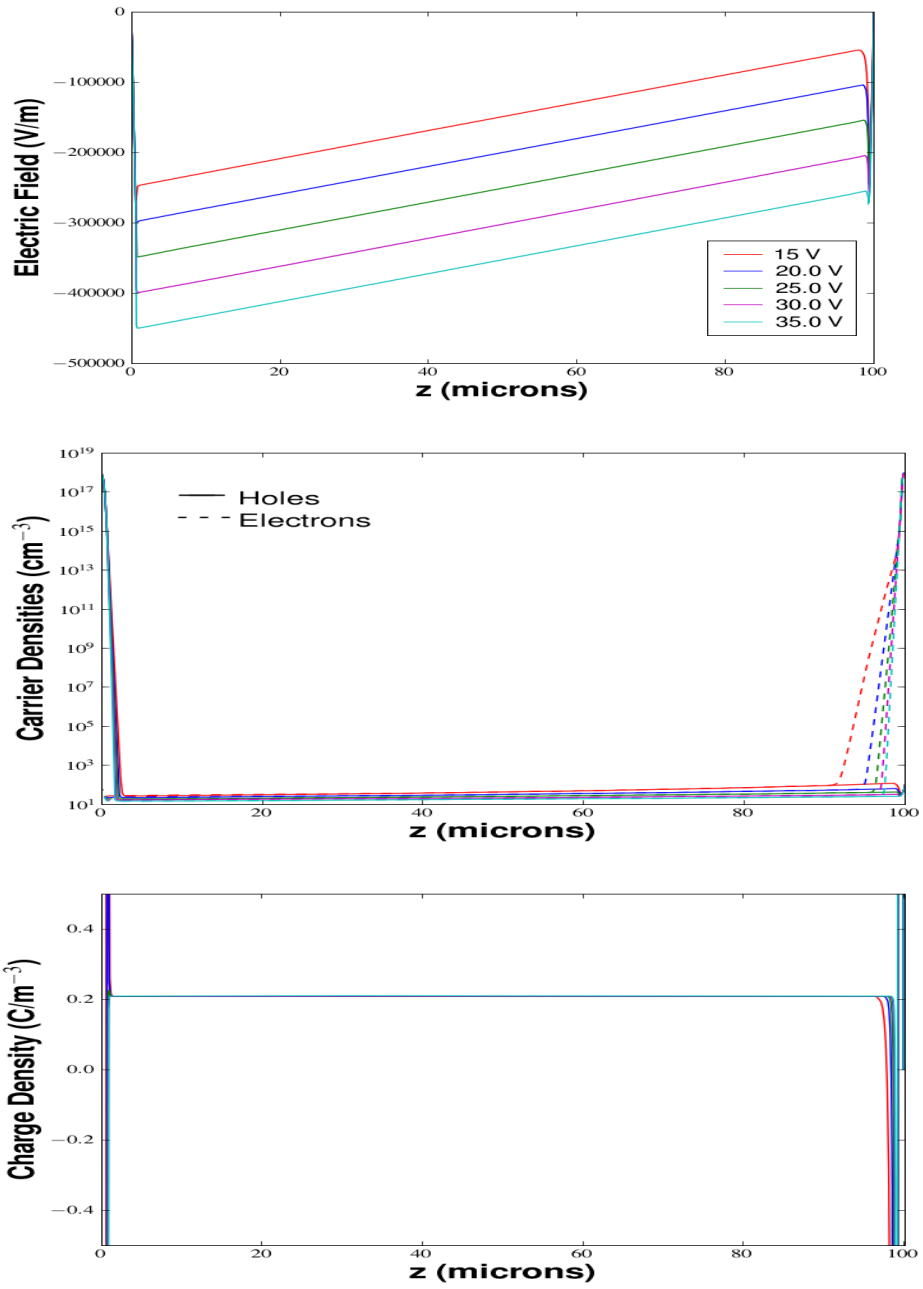

Figure 2.7: Simulated electric field (top), carrier densities (middle), and charge density (bottom) in the HyViSI PIN diodes. For most voltages shown the bulk is overdepleted. All quantities were obtained through the numerical simulations described in Appendix C.

2.2.2 The HyViSI Pixel

As seen in Figure 2.4, a full HyViSI pixel consists of **1)** the PIN diode in the detector layer and **2)** the FETs and silicon layer in the ROIC, as well as the indium bump bond and SiO_2 layer that separate the two. In presenting the aspects of the HyViSI pixel, we will first consider the capacitances associated with its various components and then study how signal is generated and eliminated.

2.2.2.1 Pixel Capacitance

To this point we have only considered the PIN diode as a two-terminal device with its ends held at fixed potentials. However, in the bulk of the HyViSI detectors, the p^+ side is actually in contact with an indium bump that connects to the input of a readout node. As mentioned earlier, this node can be the pixel of a CCD or CTIA, DI, or SFD CMOS array. In our case, the readout node is the gate of a source follower in the unit cell of a source follower per detector (SFD) CMOS array. A mock schematic of the SFD pixel is shown in Figure 2.8.

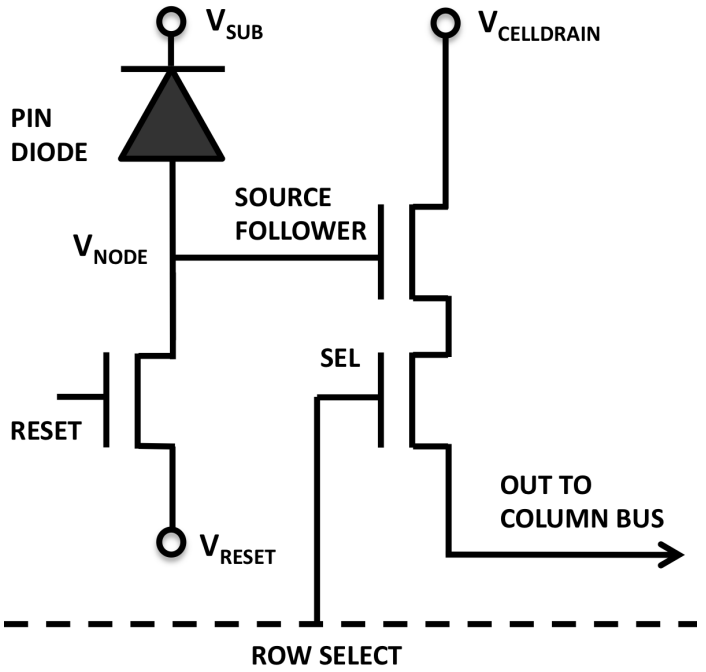

Figure 2.8: A mock schematic of a full HyViSI pixel showing the PIN photodiode in the Silicon detector layer and transistors in the ROIC. The voltages V_{SUB} and V_{RESET} are used to bias the photodiode. $V_{CELLDRAIN}$ is the drain voltage of the source follower. V_{NODE} is the effective signal that is measured through the amplification stages present in the pixel source follower and the output source follower, if it used. The select transistor allows the pixel to be addressed so that its output is placed on the column bus and eventually fed to the detector output.

The operation of this configuration is quite simple if we model the PIN diode in the bulk as a parallel plate capacitor. There are many problems with this simple model, especially in the case where the bulk region is not depleted. But it will be presented here, along with some refinements, as a starting ground for understanding how the pixels are reset and how signal is generated in the detector. The basic sequence with this model assumed is shown in Figure 2.9.

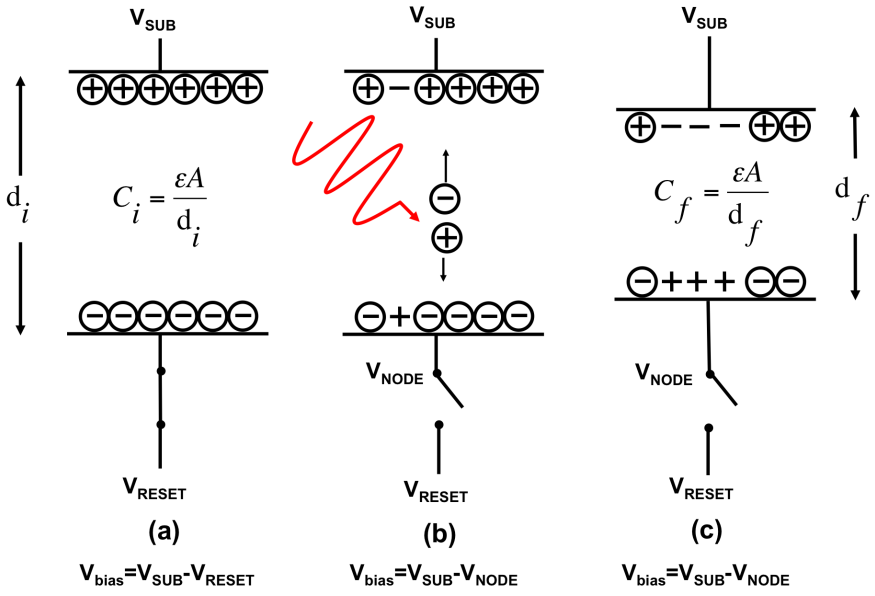

Figure 2.9: A HyViSI PIN diode pixel modeled as a capacitor. In (a) the reset switch is closed and the capacitor charges. In (b) the switch is closed and the pixel is allowed to integrate photocurrent. As V_{bias} shrinks (c), the plates of the capacitor get closer together and the capacitance grows.

Before starting an exposure, the reset switch in the multiplexer unit cell is closed, as shown in (a) of Figure 2.9. This allows the capacitor to fill up with negative (positive) charge on the bottom (top) and brings V_{Bias} to a maximum. To make the model a little more tangible we can envision electrons entering from the source of the reset transistor and filling the holes in the p+ implant and electrons exiting the n+ node through the upper contact, leaving vacant holes there. The capacitance in this case is determined purely by the geometry:

$$C = \frac{\epsilon A}{d_i}, \tag{2.5}$$

where A is the area of the pixel, ϵ is the dielectric constant of silicon, and d_i is the initial distance between the plates. We assume d_i to be the full 100 μm thickness of the detector substrate at this stage. The total charge stored on the capacitor is thus $Q_i = C_i V_{Bias}$. Ideally, we should have

$$V_{Bias} = V_{SUB} - V_{RESET} \tag{2.6}$$

However, in practice each pixel has its own small voltage offset. These offsets are of no great consequence, though, since they can be removed by subtracting a bias frame or subtracting successive reads of the detector.

After we are done resetting, the switch is opened as in (b) of Figure 2.9. Any minority carrier holes

generated, either thermally or through photo-excitation, in the bulk n material will be accelerated downward by the electric field and swept towards the p^+ implant. Once at the p^+ implant they become majority carriers. Since the probability for them to recombine with electrons in the implant is very low, they will collect there at a rate that is proportional to the number of photons impinging on the bulk. There will also be holes collected there as a result of leakage currents at the surface as well as generation-recombination (G-R) and diffusion currents in the bulk. As the holes accumulate the capacitor discharges. V_{NODE} rises and V_{Bias} decreases. The voltage V_{NODE} is what we attempt to measure to determine our signal.

As more and more carriers are collected, the depletion width of the diode will effectively decrease. In our capacitor model, this corresponds to a decrease in the distance between plates, as in (c) of Figure 2.9, and in turn, an increased capacitance. This changing capacitance can lead to non-linearity in the response of hybrid detectors, as shown by the following equation:

$$dQ = CdV + VdC. \tag{2.7}$$

In a real (ideal) parallel plate capacitor the second term would be zero since $dC = 0$. But for the PIN Diode, the capacitance changes as

$$dC = -\frac{\epsilon A}{\mathrm{d}^2} d\mathrm{d}, \tag{2.8}$$

or

$$\frac{dC}{C} = -\frac{d\mathrm{d}}{\mathrm{d}}. \tag{2.9}$$

For many hybrid CMOS detectors that use simple pn junctions as photodiodes, dC/C can be quite large. However, for the HyViSI PIN diodes this change is quite small.

The reason why dC/C is small has to do with the fact that the total capacitance of a pixel is actually the sum of several different capacitances in the detector and ROIC:

$$C_{TOT} = C_{PIN} + C_{SF} + C_{Stray} + C_{IP}. \tag{2.10}$$

where

- C_{PIN} is the depletion capacitance of the silicon PIN diode, which we estimate with Equation 2.5.
- C_{SF} is the capacitance of the source follower transistor in the multiplexer to ground.
- C_{IP} is the interpixel capacitance.
- C_{Stray} accounts for stray capacitances in the detector or ROIC.

For HyViSI PIN diodes, we find that $C_{PIN} \sim$ 0.02-0.35 fF, depending on how much of the 10 or 18 μm pixel might be occupied by the p^+ implant, while measurements show that $C_{TOT} \sim 14$ fF.

2.2.2.2 Photocurrent and Signal Generation

As the name implies, the purpose of a photodetector is to detect photons. The HyViSI accomplishes this by turning electron-hole pairs, which are produced at a rate G_e in the silicon layer, into a photocurrent, I_{PHOTO}. As shown in Figure 2.10, I_{PHOTO} is accompanied by two unwanted currents: the dark current, I_{DARK}, and persistence current, $I_{PERSIST}$. All three of these currents integrate on the capacitance C_{TOT}. The latter two will be covered in detail in later chapters; here we are only concerned with I_{PHOTO}.

We begin by assuming there is some flux of photons, Φ_o, incident on the n^+ side of the detector (originating from the right in Figure 2.5). For simplicity we will assume the photons are monochromatic with wavelength λ, and that they all have the same absorption depth, $\alpha(\lambda)$. Assuming Φ_o accounts for any photons reflected at the surface and the quantum efficiency is $\eta(\lambda)$, the rate of electron-hole production at a given depth in the detector is:

$$G_e(\mathrm{z}) = \Phi_o \alpha \eta \exp(-\alpha \mathrm{z}), \tag{2.11}$$

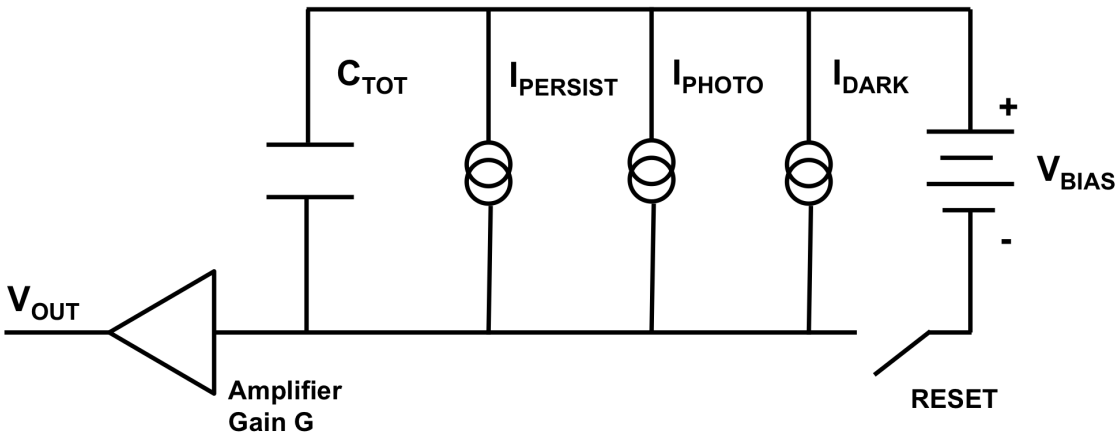

Figure 2.10: A circuit equivalent for the HyViSI pixel with source follower readout (following Figure 8.11 in McCaughrean [41]). The capacitance C_{TOT} is the one listed in Equation 2.10. I_{PHOTO} is the photocurrent, I_{DARK} is the dark current, and $I_{PERSIST}$ is current generated from persistent charge. V_{BIAS} is the bias applied to the diode at reset and V_{OUT} is the voltage sensed through the amplification, G, that results from the source followers in the signal path.

where we have taken the back surface as z=0 and the direction moving into the diode as the positive z direction. Gärtner uses this expression to solve for the total current density, J_{tot}, through a one-dimensional PIN diode [58]. However, he makes the crucial assumption that the electric field through the diode is constant. It is clear from Figures 2.6 and 2.7 that the electric field in the HyViSI PIN diodes is not constant, which renders the analysis invalid for them.

It is especially important to consider cases where the diodes are not fully depleted since there will be regions completely free of electric field, and carriers generated in these regions will contribute to a lateral current in the x, y directions. For bulk regions where there is a nonzero photon flux and electric field, the drift current is given by

$$J_{drft} = -q \int_0^{W_D} \left[G_e(\mathrm{z}) + \Delta p_{diff}(\mathrm{z})\right] E(\mathrm{z}) \mu_p d\mathrm{z}, \tag{2.12}$$

where μ_p is the mobility of holes, $E(\mathrm{z})$ is the electric field along the length of the diode, and W_D is the width of the depletion region. Δp_{diff} represents any of the free holes that have diffused into the pixel field, either from a photogeneration site directly above the depletion region or from the field free region of a neighboring pixel.

The diffusion of holes from an illuminated pixel to its neighbors can happen quite easily when the detector is not overdepleted since the accumulation of photocurrent actually causes the depletion region in the illuminated pixel to collapse. When holes drift to the front surface and recombine with the ionized acceptors, W_P in Figure 2.1 shrinks; the same happens for W_D when electrons drift to the back surface. This leads to an increase in the undepleted width ΔW_U^{lum} for the illuminated pixel. In the neighboring pixels, no such reduction of W_D has occurred. Hence, any of the diffusing carriers in the newly formed ΔW_U^{lum} that migrate laterally will find themselves directly in the depletion region of a neighboring pixel and contribute to its drift current through the term Δp_{diff}. Eventually, the depletion regions of the neighboring pixels will collapse as well, allowing holes to diffuse and be collected by pixels beyond. An example of this, which is known as "blooming" in imager speak, is shown in Figure 2.11.

The holes which are collected by the electric field accumulate as majority carriers in the p^+ implant and are stored as signal charge, $Q(t)$:

$$Q(t) = -qA \int_0^t \left(\int_0^{W_D} \left[\Phi_o \alpha \eta \exp(-\alpha \mathrm{z}) + \Delta p_{diff}(\mathrm{z})\right] E(\mathrm{z}) \mu_p d\mathrm{z} \right) d\mathrm{t}. \tag{2.13}$$

The integration of Q does not go on indefinitely; this equation is only valid until the potential well in the p^+ region has filled up to the full well, $Q = Q_{FW}$ (see Section 6.1.4.3 for a discussion of diffusion at the front surface). Because of the field free region, there will also be a large number of excess minority carriers in the bulk. The number of minority carrier holes present in a given pixel will depend on the number generated by incident photons, Δp_{lum}, the net difference between holes diffusing in

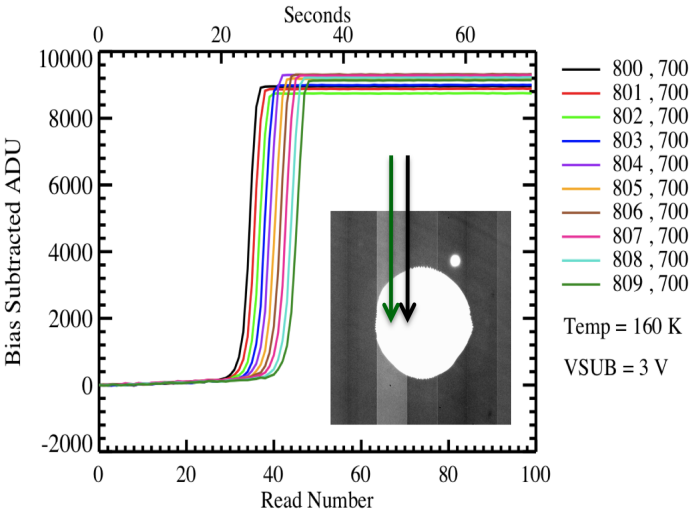

Figure 2.11: This plot shows the signal vs. time (after subtraction of bias offset) for a set of pixels that have received holes from strong lateral diffusion in the undepleted region of H1RG-022. At first they integrate only a small flux from the sky, Φ_o^{sky}. Once the depletion regions in their right neighbor pixels have collapsed they see a huge jump in signal due to the hole diffusion, Δp_{diff}. The raw image from which these ramps were taken is shown in the inset.

and diffusing out, Δp_{diff}^{net}, and their lifetime, τ_p, as they recombine. Unfortunately, as seen in Figure 2.11, the output of the detector is railed by the 3.3 V upper limit of the CMOS multiplexer, making it difficult to fold in the lifetime of the carriers.[3] The exact doping and geometry in the detector material is not known either, which presents another difficulty. But it is still worthwhile to make a semi-quantitative analysis of the expected distribution of holes in the underdepleted state. The sum of collected holes and free minority holes should get smaller with distance away from the center of illumination, and we can designate four separate radial regions based upon the constituent sources of holes:

$$p = \begin{cases} Q_{FW} + \Delta p_{lum} - \Delta p_{diff}^{net} & 0 < r < r_1 : \quad \text{Saturated by Illumination} \\ Q_{FW} + \Delta p_{diff}^{net} & r_1 < r < r_2 : \quad \text{Saturated by Diffusion} \\ Q(t) + \Delta p_{diff}^{net} & r_2 < r < r_3 : \quad \text{Integrating Diffused Holes} \\ 0 & r_3 < r \quad : \quad \text{Outside Diffusion Envelope} \end{cases} \tag{2.14}$$

If we are considering point sources of light, r_1 should be about the 1.5-3 $\times$ the FWHM of the star. Outside of r_1, the pixel wells fill up purely because of the holes that diffuse to their depletion regions. At some radius r_2, the wells have just begun to collect diffused holes (one can see r_2 moves outward with time in Figure 2.11). And outside of a radius r_3, the diffusion has not yet reached the pixels, so they are integrating only dark current. It should be noted that **these regions are only relevant for the underdepleted case** (when overdepleted, there is very little measurable diffusion). Still, they will be extremely important in analyzing image persistence in Section 7.2.

[3] In a detector where the output did not rail at some voltage, V_{rail}, we would be able to see a gradient in the signal vs. position. This gradient would allow us to solve the diffusion equation for the diffusion coefficient, D_p, and lifetime, τ_p. But because $V_{rail} = 3.3V$, we are only sensitive to the small range of signal and the gradient is masked.