Testing and Operation of the SIDECAR ASIC for DUNE and LSST

Lance M. Simms [a], Steven M. Kahn [a], D. Kirk Gilmore [a], Suresh Seshadri [b]

[a]Stanford Linear Accelerator Center, Menlo Park, CA, 94025 USA;
[b]Jet Propulsion Laboratory, Pasadena, CA, 91109 USA

ABSTRACT

We report on laboratory testing and performance measurements of the Teledyne Scientific SIDECAR ASIC using working parameters intended for the H1RG and H2RG multiplexers. We show that the pre-amplifier kTC noise cancellation and multiple channel averaging modes reduce electrical noise as expected and investigate the behavior of the noise with decreasing analog-to-digital conversion time. Gain measurements and working bias currents are provided along with a list of possible sources of instability in the successive approximation ADCs.

1. READOUT ELECTRONICS: SIDECAR ASIC

Interfacing focal plane arrays (FPAs) to a data acquisition system (DAQ) in astronomy usually requires a middle-man set of electronics that are referred to as the "readout" or "control" electronics. The readout electronics handle tasks such as converting the analog video signals to digital numbers, filtering noise from the signals, providing power or bias voltages to the FPA, and generating the clocking signals necessary to take an exposure with the array. In many cases this set of electronics is equipped with a microprocessor or microcontroller that can store a set of instructions in its internal memory. Different sets of instructions can be loaded based upon the desired mode of operation for the FPA (i.e. binning pixels, reading a subset of the array, etc.). And with a given set of instructions loaded, writing individual registers allows for fine tuning of parameters such as the frame rate and exposure time.

In most cases these readout electronic systems are rather bulky. Large racks are often needed to hold them and the power supplies that they need to operate. In some cases the readout electronics draw enough electrical current from the supplies to necessitate a fan to prevent overheating. They typically consist of multiple circuit boards with discrete chips for each function, i.e. voltage regulators, DACs, ADCs, memory etc. Often times, to make slight adjustments, additional components such as resistors or capacitors must be inserted or soldered to the boards. Since these electronics are in most cases bolted to a telescope or flying on a satellite in astronomical applications, weight and size can be an issue, and certainly one would rather avoid swapping out components.

To step away from the bulkiness and large power requirement of traditional electronics, Teledyne Scientific has produced a multi-purpose control application-specific integrated circuit (ASIC) called the SIDECAR (**S**ystem for **I**mage **D**igitization, **E**nhancement, **C**ontrol **A**nd **R**etrieval Application). A block diagram of the SIDECAR ASIC and photographs of the 22 x 14.5 mm^2 die mounted in two different packages is shown in figure 1. As the diagram indicates, the chip contains all of the functionality needed to control and readout a detector: clocks, biases, ADCs, etc. And in addition to the functions shown, the chip provides pre-amplification and amplification stages as well as array processors that permit data processing function such as co-adding channels or subtracting offsets.

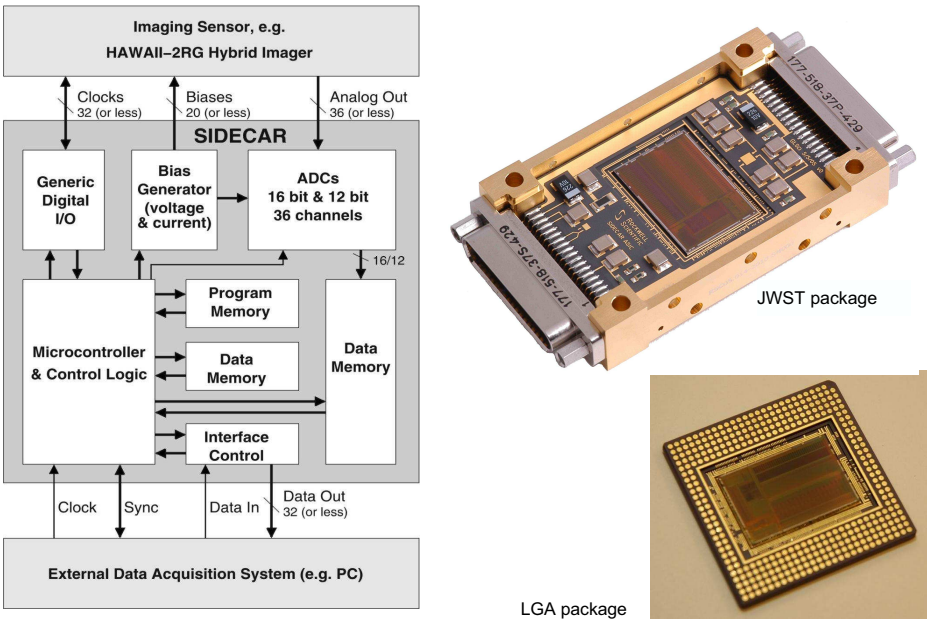

Figure 1. A block diagram of the SIDECAR ASIC along with two packaging options available for the chip (taken from Ref. 1).

In addition to the compact science mission packaging schemes shown in figure 1, Teledyne offers the SIDECAR in a development kit intended for laboratory use. The development kit, which was used for all measurements included in this report, is shown in figure 2. In this configuration, the ASIC is placed on a board that has numerous test points that allow one to probe its various output signals and LEDs that show clock activity. This board connects to a smaller board called the JADE card that handles communication with a Windows PC via a USB interface. The development kit as a whole is essentially a plug and play device. The user only needs to write the assembly code instructions for the microcontroller in the ASIC and the software that the PC will use to extract the data through the USB bus. For the latter, a library of Microsoft COM functions is provided so that typical astronomy applications such as IDL can be used for data retrieval and configuration.

It should be mentioned that Teleldyne offers the SIDECAR Development Kit in two flavors: warm and cold. The warm kit operates at room temperature, and so it must be placed outside the cryogenic system enclosing the detector to which it is attached. This implies that there is a significant length of cable over which the analog signals must travel between the ASIC and the detector. We have only tested this type of kit. The cold kit can operate at cryogenic temperatures, which means that it can be placed directly beside the detector so that only digital signals going to and from the DAQ must travel over long distances. We suspect that noise pickup over the analog cables along with the temperature of the chip itself will make the noise higher in the warm kit, and we hope to have the chance to test the cold kit in the future to verify this. However, the basic operation of the chip should be the same in both kits, and most of the

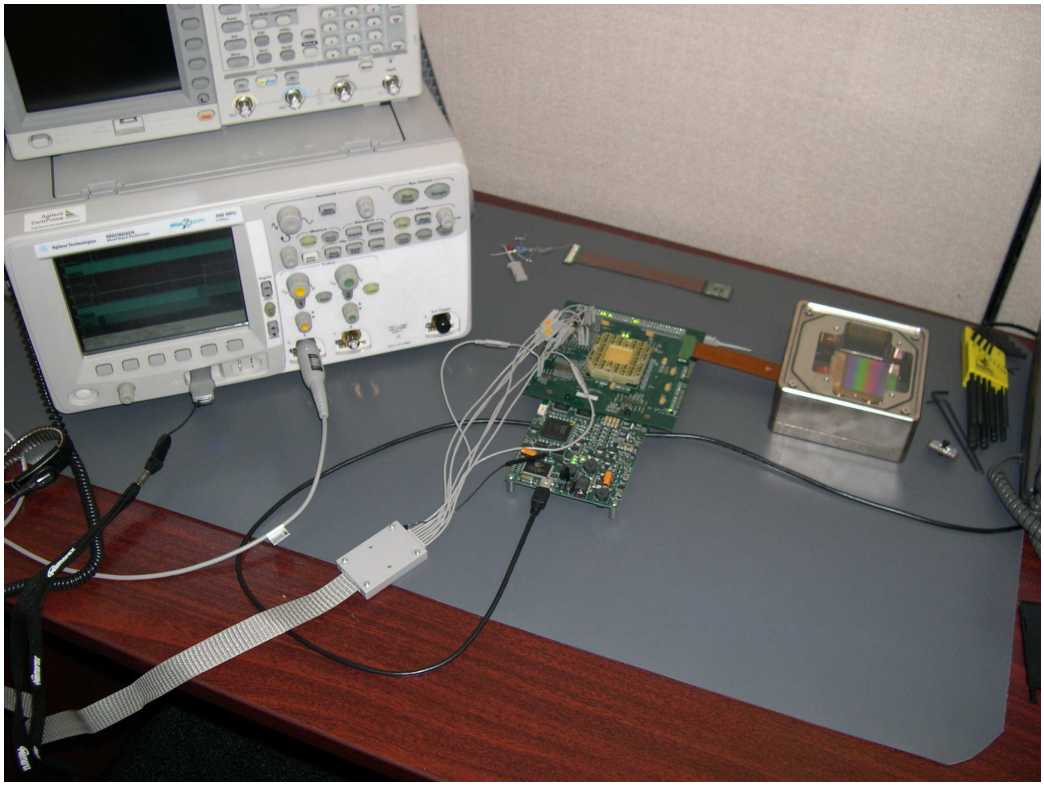

Figure 2. A photograph of the SIDECAR development kit attached to an H4RG multiplexer and a USB cable going to a laptop computer not shown. Multiple clocks and analog signals are being traced on the oscilloscope.

material in this report should be applicable to either one.

In the following sections we will not provide a comprehensive description of the chip; only a brief review of some of the features and its performance in the various modes of operation with the HyViSi devices. For a detailed description of the SIDECAR, the reader is referred to Refs. 1 and 2.

2. PRE-AMPLIFICATION STAGE

Before analog-to-digital conversion takes place, the video signals from the detector are first fed into the SIDECAR pre-amps. In the pre-amp stage, signals can be routed to different channels or shared among them via an internal mux, offsets can be added to them with a DAC and they can be amplified and filtered. The amplifcation sub-block of the pre-amps, displayed in figure 3, shows that capacitive feedback is used for gain selection with the capacitors C_{FB} and the inputs are capacitively coupled to the amplifier through C_{IN}. Capacitive feedback has the advantage that is does not lower gain since it does not trade gain for bandwidth.[3]

During the amplification stage, the switches $S3$ and $S6$ are open. This leaves the nodes of the capacitors C_{FB} floating at a potential set by a reset transistor switch. As mentioned in Ref. 1, inevitable leakage currents in the silicon will cause these nodes to drift with a time constant that depends highly on temperature. When the SIDECAR chip is placed inside the dewar and cooled along with the detector, the leakage currents are very small and this does not present a problem. However, when the SIDECAR is held at room temperature, the pre-amp drifts are

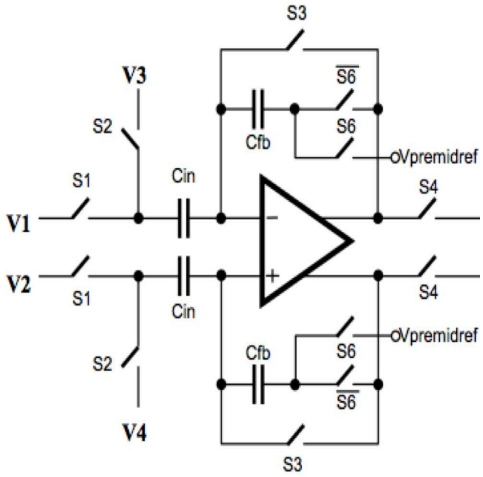

Figure 3. A schematic of the amplication stage for a given channel in the SIDECAR taken from.[2] Note that capacitors are used for feedback rather than resistors.

very noticeable after fractions of a second. This drift and the noise associated with resetting the capacitors take different forms based upon the implementation of the signals available in the pre-amp stage.

Pre-amp reset once per frame From the standpoint of assembly coding, an easy-to-implement conversion sequence is to reset C_{FB} once per frame. However, for frame times as short as 0.25 seconds, the leakage currents can cause the output voltage going into the ADCs to swing by as much as 25 mV. This drift over the frame, which will continue for longer frame times, is shown in the top of figure 4. It is evident then that more frequent resets of the pre-amp capacitors are needed at room temperature.

Pre-amp reset once per row: No kTC Removal An alternative to resetting once per frame is to reset before every row conversion. The row may consist of the number of pixels in a row per output of the detector or the number of pixels in the row of a sub-window. The problem with this is that after each reset, a random amount of charge will be left on C_{FB}. The noise associated with this random charge should be proportional to kTC_{FB}, where k is Boltzmann's constant and T is the temperature. The pattern associated with this noise, shown in the middle frame of figure 4, consists of horizontal bands across the frame. And since it is uncorrelated from frame to frame, CDS subtraction of two consecutive frames will boost this noise by $\sqrt{2}$.

Pre-amp reset once per row: With kTC Removal In order to deal with the horizontal banding caused by kTC noise, an intrinsic analog CDS scheme is used in the pre-amp and ADC blocks. In each ADC conversion, both the video signal from the pre-amp and the voltage on the capacitors are sampled. The ADC digitizes the sampled signal using the latter as a reference so that the kTC offset subtracts out. The last frame in 4 shows that the noise is essentially white when this method is used. The implementation of the kTC removal scheme involves toggling one signal in the pre-amp and slightly changing the internal bias voltages from those used in the normal reset schemes; it does not require additional time for conversions.

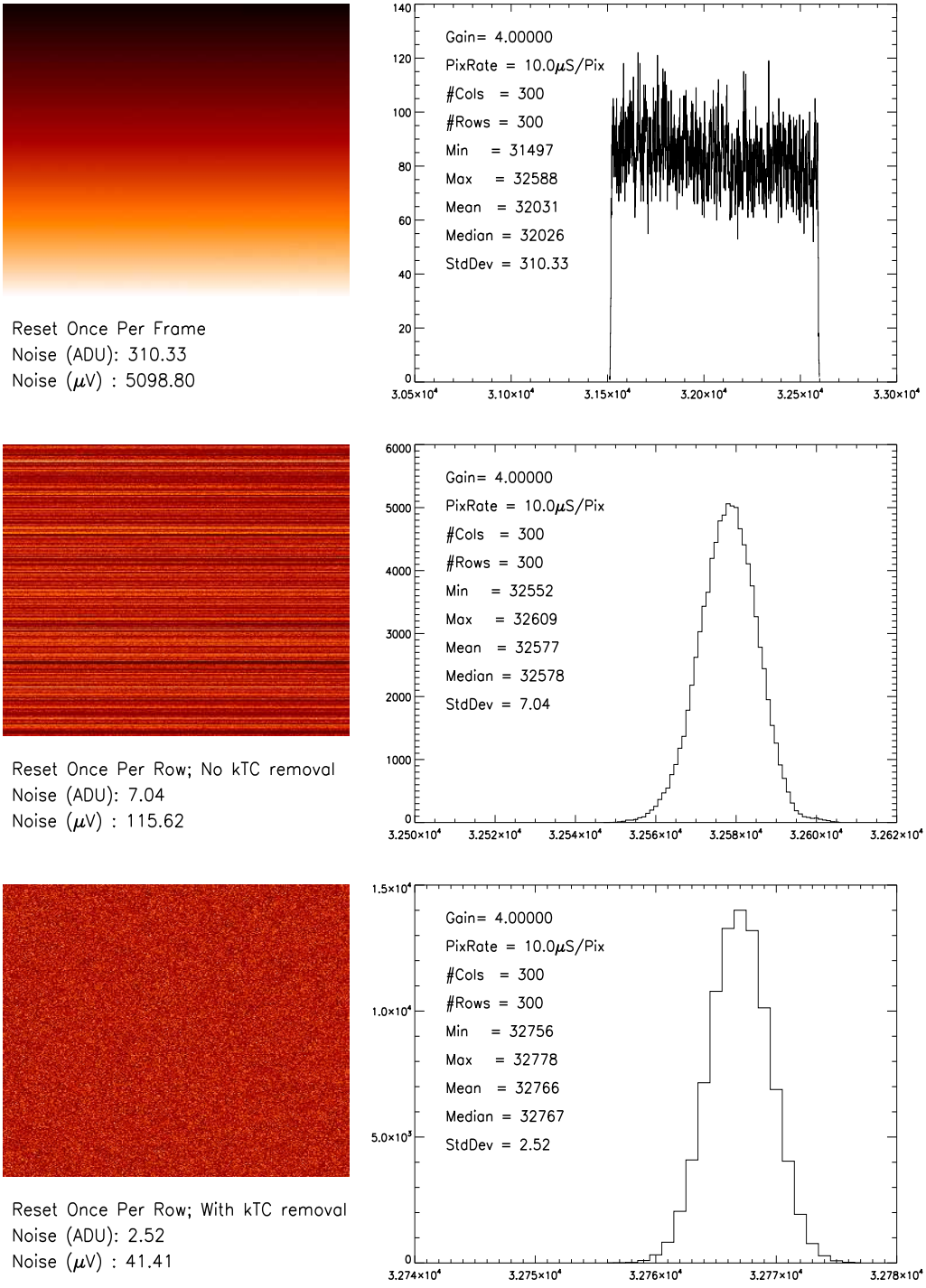

Figure 4. Different reset schemes for the SIDECAR pre-amps. All measurements were made with the input voltages $V1$-$V4$ connected to the internal ground.

3. CONVERSION GAIN

In all measurements described in this report, the 16 bit Successive Approximation (SAR) ADCs were used. For the SAR ADC, the conversion from microvolts to ADU is given approximately as

$$Counts(ADU) = 32768 * \frac{V_{In} - V_{Ref}}{VRP - VRN} * G + 32768, \quad (1)$$

where V_{In} is the input voltage to the pre-amp, V_{Ref} is one of the selectable reference voltages provided on the chip, VRP and VRN are ADC reference voltages, and G is the gain of the pre-amp. G is configurable in $3dB$ increments from -$3dB$ to $27dB$. V_{In} and V_{Ref} correspond to the input voltages $V1$ and $V2$ in figure 3.

To obtain a conversion from voltage to ADU and measure the actual values of G for our configuration, a voltage was supplied to the pre-amp inputs with an Agilent E3647A Dual Output 30 volt power supply. This voltage was increased from 0-3.3 V by 0.1 V increments and at each increment a set of 20,000 digitizations were recorded. The mean of these digitizations were taken to yield an average ADU value at that voltage. The conversion from μV to ADU at a gain of 1 is shown in figure 5. The conversion measured at other gains is listed in table 1.

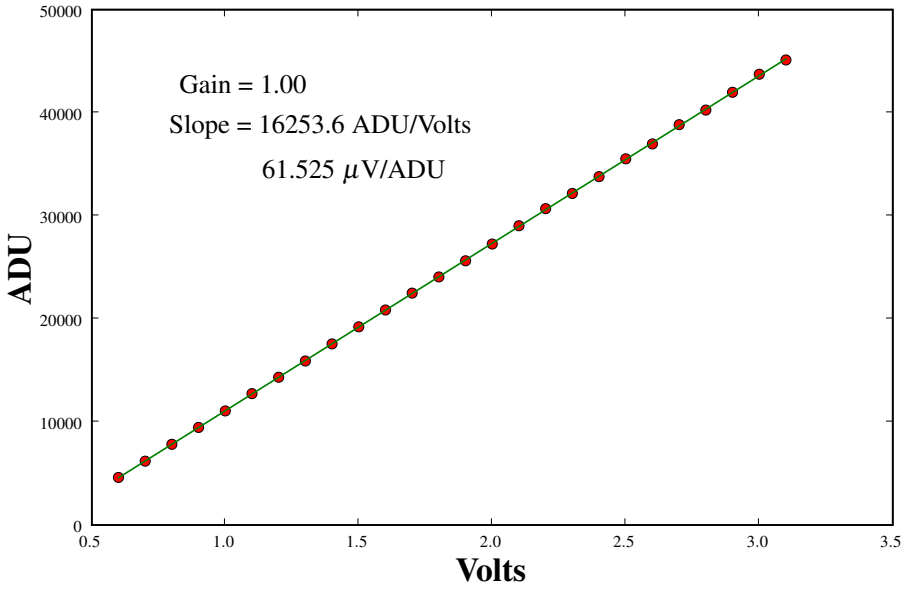

Figure 5. Average digital ADU values (shown as red dots) vs. the input voltage at which they were measured. The inverse slope of the best-fit line (shown in green) to the points yields the conversion in μV/ADU.

Table 1 shows that as the gain setting in the pre-amp is increased, the measured gain moves farther from the expected value, with the former being less than the latter. This is due to the use of low noise resistors and single-stage buffers in the system. As indicated in Ref. 2, low noise settings result in diminished gain. However, the measured values are very repeatable, so with proper calibration this discrepancy can be taken into account and should not be a performance-limiting issue.

The last two columns in the table labeled *Ground Noise* show the digitization noise when the pre-amps are configured to measure the internal ground signal of the chip. In agreement with figure 5 in Ref. 1, the noise is ADC limited below a $G = 4$ and above that it is limited by the pre-amp. The two columns labeled *Supply Noise* contain the ditization noise measured when reading the voltage from the Agilent power supply. The RMS output noise of the power supply was measured with an oscilloscope to be about 340 uV, so this asymptotic behavior of the noise with increasing gain is to be expected.

Table 1. Measured pre-amp gains for the SIDECAR ASIC

Gain	Gain (dB)	Measured Gain (uV/ADU)	Measured Gain	Supply Noise (ADU)	Supply Noise (uV)	Ground Noise (ADU)	Ground Noise (uV)
0.71	-3.01	86.07	0.71	4.79	412.3	2.70	232.4
1.00	0.00	61.53	1.00	6.81	383.9	2.72	166.7
1.41	3.01	43.56	1.41	8.35	363.7	2.78	121.1
2.00	6.02	30.77	2.00	11.67	359.1	2.80	86.2
2.83	9.03	22.96	2.83	16.22	352.4	2.75	59.7
4.00	12.04	15.46	3.97	22.52	348.2	2.81	43.4
5.65	15.05	11.01	5.58	31.10	342.4	2.97	32.7
8.00	18.06	8.01	7.67	43.03	344.6	3.22	25.8
11.31	21.07	5.75	10.71	59.90	344.2	3.62	20.8
16.00	24.08	4.15	14.84	83.82	347.2	4.29	17.8
22.62	27.09	3.00	20.48	115.01	345.9	5.25	15.8

4. AVERAGING MULTIPLE CHANNELS

The input routing multiplexer of the pre-amp and math capabilities of the array processor (AP) allow one input signal to be shared and digitized on multiple channels and then averaged before it is written to the dual port memory and read out by the DAQ. This might be advantageous if buffer size or memory overflow is an issue in the readout system. And this feature is particularly useful for the HxRG multiplexers as the number of outputs is configurable. For instance, the detector can be run in four output mode, with each output being sampled and averaged between eight channels on the SIDECAR. And in window mode only one output of the detector is used, so there is no reason not to take advantage of multiple channels on the SIDECAR.

Each math operation and read/write in the array processors requires at least one clock cycle. One would expect that doing math between A/D conversions would therefore result in an overall slower pixel conversion time. However, the array processor clock can be configured to run at a faster rate than the ADC clock so that no time is lost between successive A/D conversions [*]. Example clock rates and conversion times are given in table 2. The redundancy is meant to illustrate that no decrease in pixel rate is suffered.

The basic process for averaging N channels is as follows: The first channel writes its value to dual port memory. After a certain delay, the second channel reads this value from memory, adds its own A/D value to it, and writes it back to the same address. This process continues with the N channels until all have been coadded. Then a bit shift (or a multiplication followed by a bit shift for the case of $N = 6$) is used to acheive the averaging. Finally, the value is written back to memory and stored until it is extracted by the DAQ.

Table 2. SIDECAR clocking scheme for averaging multiple channels

Channels	System Clock (MHz)	AP Clock (MHz)	ADC Clock (MHz)	AP Cycles / Pixel (Used/Total)	ADC Cycles / Pixel (Total)	Pixel Time (μS)
1	10	1.00	1.00	2/10	10	10
2	10	1.00	1.00	5/10	10	10
4	10	5.00	1.00	13/50	10	10
6	10	5.00	1.00	17/50	10	10
8	10	5.00	1.00	24/50	10	10

Figure 6 shows the reduction in noise when multiple channels are averaged. The decrease goes nearly as the theoretically predicted $1\sqrt{N}$ channels, indicating that the noise in the ADCs is uncorrelated.

[*]The only caveat is that the ADC clock must be divided relative to the AP clock. Since both clocks are derived from the microcontroller system clock, the ADC clock must run more slowly than the system clock if more than 2 channels are averaged. See table 2 for the relative rates.

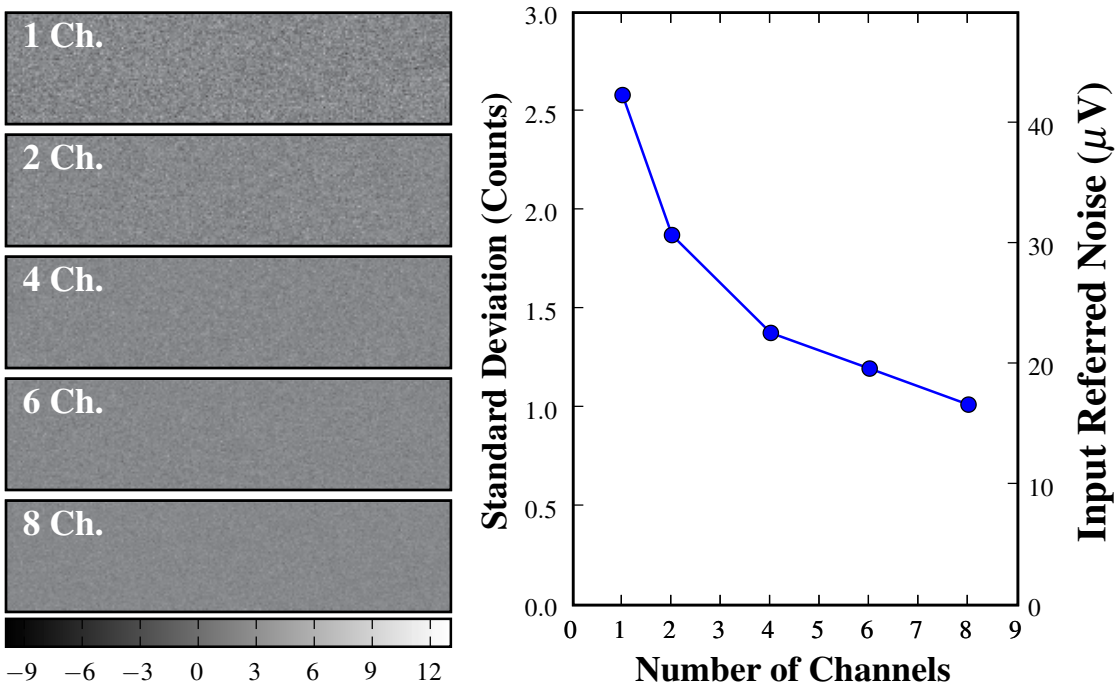

Figure 6. (left) Digitizations of noise in the SIDECAR for 1-8 channels at a pre-amp gain of 4. The colorbar shows the ADU values after subtraction of the mean value of 32768. (right) The RMS value of the noise as a function of the number of channels averaged.

Application to H1RG HyViSi Detector As an example of the usefulness of averaging multiple channels and selecting the proper conversion gain on the SIDECAR, temporal read noise measurements were made on the 1024x1024 Hybrid Visible Silicon (HyViSi) detector H1RG-022. To make these measurements we ran the detector in window mode and obtained a set of correlated double sample (CDS or *reset-read-read*) frames. The window selected included the first 100 rows and 100 columns of pixels. The first 4 rows and first 4 columns of the window were reference pixels that have a capacitance of roughly $C_{Ref} = 35\ fF$ and all of the others were science pixels that have a capacitance of $C_{Sci} = 14\ fF$. After obtaining a stack of CDS frames, we look at the temporal variation of each pixel and measure its standard deviation. Averaging the standard deviations yields the temporal read noise.

As illustrated in figure 7, the difference in pixel capacitances makes a significant difference in the read noise, especially when measured in electrons. In astronomical applications, quantifying the read noise in electrons is the most useful since this is the quantity that can be directly used, along with quantum efficiency, to estimate the number of photons that hit a given pixel. We see that for small capacitances, the larger gain yields a much smaller read noise in electrons. For the eight channel average noise of the reference pixels, both measurements yield a noise of about 3 ADU, indicating that the ADC contribution to the noise might be dominating rather than the contribution from the detector noise.

The lower read noise at higher gain is very desirable, suggesting that the SIDECAR pre-amps should be run at a high gain with HyViSi detectors. However, one must also consider the trade-off between gain and the usable dynamic range of the detector. For instance, in the case of H1RG-22 the well depth is approximately $110,000\ e^-$. If the SIDECAR pre-amps are set at a gain of 4 the conversion gain is about $1.4\ e^-/ADU$ and the full ADU range needed to cover the entire well will be 78,500 ADU. However, the 16 bit ADC allows a maximum of 65,536 values, so some portion of the voltage range will be lost. If the entire well depth is to be used, a gain slightly below this must be chosen.

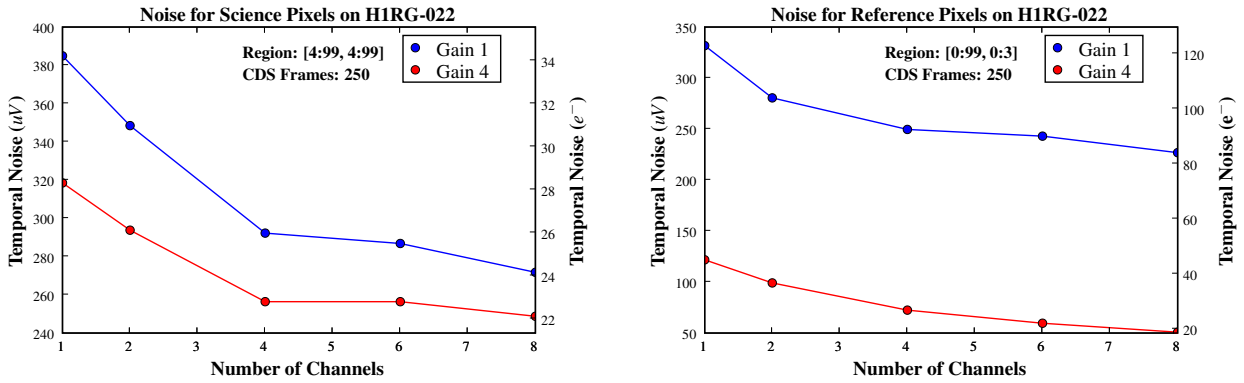

Figure 7. (Left) Read noise of H1RG-022 science pixels measured with multiple channels averaged. (Right) Read noise of H1RG-022 reference pixels measured with multiple channels averaged. The capacitance of the science pixels is roughly 2.5 times as large as that of the reference pixels. For this particular measurement, the SIDECAR was configured so that $G = 1$ yielded 64 uV/ADU and $G = 4$ yielded 16 uV/ADU.

5. NOISE PERFORMANCE VS. PIXEL TIME

Among other projects, the SIDECAR is being considered for use in the guider cameras of the **L**arge **S**ynoptic **S**urvey **T**elescope (LSST) and the **S**uper**N**ova **A**cceleration **P**robe (SNAP). An important parameter for both of these systems will be the frame rate for imaging a guide star, which is dependent on the pixel conversion time. For 100 Hz adjustments of the telescope pointing using centroids from multiple guide stars, a pixel conversion time smaller than 10 μS may be required. And for science imaging applications, reducing the pixel time has the added benefit of increasing dynamic range since bright stars can be imaged before they saturate the pixels. The performance of the SIDECAR ADC at faster A/D conversion times will thus directly affect both of these applications.

Increasing the pixel conversion rate means that voltages in the system, i.e. the analog output of the detector, the digital clock signals, the DAC voltages used in the SAR ADC, etc., must change more quickly. The relationship $I = C\ dV/dt$ tells us that changing these voltages more quickly requires increases in electrical current. In general, increasing the speed at which signals are converted to digital output should be accomodated by an increase in drive currents in the system and an attempt to reduce source impedances and load capacitances to account for this. In the case of the SIDECAR, we need to increase the bias currents in the pre-amp and SAR ADC.

For most ground based astronomy missions, boosting the currents is perfectly fine since there is usually plenty of electrical power for the electrical and thermal systems. However, for space based missions it might be desireable to keep the currents and heat dissipation as low as possible since electrical power from solar panels is not an abundant resource. For this reason, the minimum ADC and pre-amp currents needed to operate the SIDECAR at each clock speed were sought. Values for which the noise histogram remains approximately Gaussian in shape up to a gain of $G = 4$ are listed in table 3.

If the drive currents fall significantly below these values, certain instabilities in the digital output of the SIDECAR will result. A description of these instabilities, along with the current that is most likely lacking is included in the following section. In general, increasing the currents I_{NBIAS1}, I_{NBIAS2}, $INFB1$, and $INFB2$ will decrease the ADC noise (Markus Loose, private communication). However, if brought too high they can also cause instabilities. It should also be mentioned that the values listed in table 3 work for gains less than or equal to $G = 4$. If a higher gain is used, one or more of the currents may need to be increased.

Additional Notes

- Noise histogram is very sensitive to DAC buffer current of VRP and VRN.
- The most important settings in determining the RMS and the shape of the noise histogram seem to be $I_{PreAmpBias}$. If $I_{PreAmpBias}$ is too low, the noise will be high and at a certain threshold, the histogram will take a pitchfork shape like that in middle panel of figure 8.
- When we increase the pre-amp gains, we should also increase I_{NBIAS1}, I_{NBIAS2}, I_{NFB1} and I_{NFB2}. Otherwise, the noise distribution becomes jagged, indicating a loss of the LSB.

Table 3. Operating parameters and noise performance at different A/D sampling rates on the SIDECAR ASIC. Note that the noise can be kept at a nearly constant level below 167 kHz by increasing the bias currents.

Sampling Rate	100 kHz	125 kHz	167 kHz	250 kHz
$I_{PreAmpBias}$ (μA)	6.40	6.40	16.00	17.60
$I_{PreAmpCasc}$ (μA)	1.60	1.60	1.60	1.60
I_{NBIAS1} (μA)	11.30	14.50	17.70	48.00
I_{NBIAS2} (μA)	11.30	14.50	17.70	48.00
I_{NFB1} (μA)	5.00	5.00	13.00	34.00
I_{NFB2} (μA)	5.00	5.00	13.00	34.00
$I_{VRP\ DAC}$ (mA)	0.343	0.343	0.343	0.654
$I_{VRN\ DAC}$ (mA)	60.00	60.00	60.00	60.00
RMS Noise (ADU)	2.65	2.65	2.76	3.13
RMS Noise uV	41.0	41.0	42.7	48.4

- If I_{NBIAS1} and I_{NBIAS2} are too small, the histogram will appear jagged, with the odd ADU values having smaller values than their even neighbors as in the top panel of figure 8.
- If I_{NFB1} and I_{NFB2} are too small, the distribution will be less strongly peaked. Increasing these currents will make the peak tighter. If these currents are too small, a gap might form in the distribution.
- Large capacitance loads will cause ringing somewhere in the ADC. The resultant histogram will have at least three separate peaks. Increasing the drive currents will bring these peaks closer together and eventually they will merge.
- The DAC buffer current for VRP should be adjusted for different gains in order to keep a nicely peaked histogram.
- If I_{NBIAS1}, I_{NBIAS2} are set too high, speckles will appear in the digitizations, indicating voltage spikes somewhere in the system, as in the bottom panel of figure 8.

6. CONCLUSION

We have tested the Warm Development Kit version of the SIDECAR ASIC and verified operation of the various noise reduction modes it provides. These include pre-amplifier kTC noise removal and averaging of one signal on multiple channels. We also performed gain measurements and examined the noise performance at increasing conversion speeds up to 250 kHz with the SAR ADCs. Assuming the noise will sum in quadrature when hooked up to an imaging detector, the contribution from the SIDECAR will likely be negligible with respect to the output noise of the detector. The SIDECAR should meet sensor performance goals when combined with H2RG NIR HgCdTe sensors, making it a good candidate for the readout subsystem in the DUNE mission.

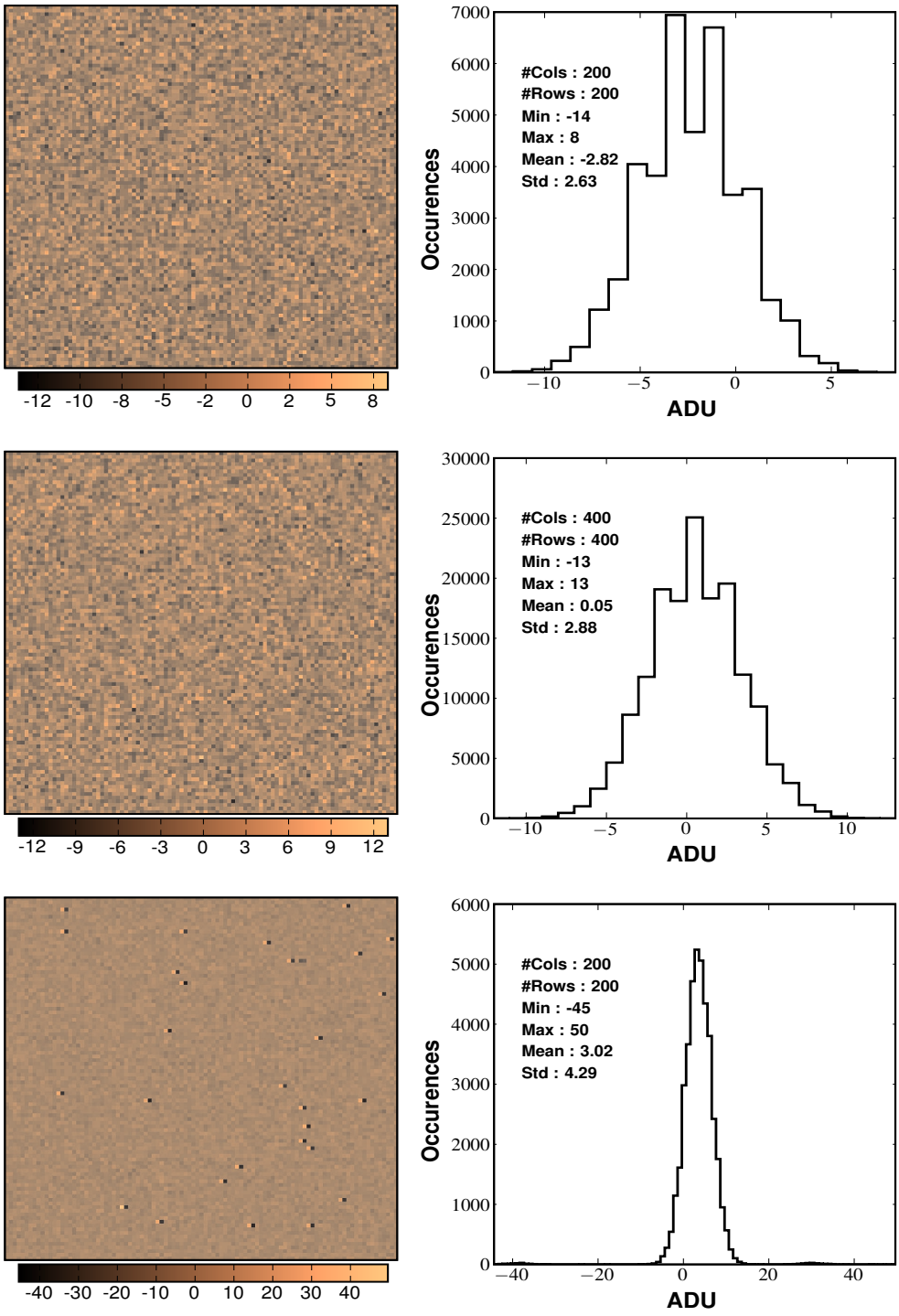

Figure 8. (Top) Digitizations taken at 8 uS when $I_{NBIAS1} = I_{NBIAS2} = 8.1\mu A$ were too low. (Middle) Digitizations taken at 6 uS when $I_{PreAmpBias} = 1.6\mu A$ was too low. (Bottom) Digitizations taken at 4 uS when $I_{NBIAS1} = I_{NBIAS2} = 53\mu A$ were too high. All digitizations were taken with $G = 4$.

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